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UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD, ET AL., Defendants.	Case No. 2:22-cv-293-JRG (Lead Case) JURY TRIAL DEMANDED [redacted]
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG (Member Case) JURY TRIAL DEMANDED **FILED UNDER SEAL**

DEFENDANTS' MOTION FOR SUMMARY JUDGMENT OF
LACK OF WRITTEN DESCRIPTION FOR U.S. PATENT NO. 11,093,417

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TABLE OF CONTENTS

[redacted]

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

Other Authorities

[redacted]

TABLE OF EXHIBITS

Ex. No.	Description
A	Exhibit C to Opening Expert Report of Dr. Mangione-Smith
B	*Netlist Inc.*, v. *Samsung Electronics Co., Ltd., et al., Markman* Hearing on September 26, 2023
C	Redline comparison of the text of the ’417 patent and its parent U.S. Patent No. 10,89,314
D	Exhibit B to Rebuttal Expert Report of Dr. Mangione-Smith
E	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)

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I. INTRODUCTION

The Micron Defendants (collectively, "Micron") move for summary judgment of lack of written description for U.S. Patent No. 11,093,417 (the "'417 patent"). The Court should grant summary judgment in favor of Micron because independent claim 1 (the only independent claim) lacks sufficient written description.

Summary judgment is warranted because the '417 patent does not provide adequate written description for the recited "CAS latency" limitation. The claims recite specific requirements for the "data transfers through the circuitry," that they are "registered for an amount of time delay such that the overall CAS latency … is greater than an actual operational CAS latency." ('417 patent, claim 1). There is no adequate written description for registering data transfers going into the memory module (write commands) "such that the overall CAS latency … is greater than an actual operational CAS latency."

Summary judgment is also warranted because the applicant added new matter to the '417 patent relating to "data buffer control signals" that was not present in prior applications in this patent family. Summary judgment on this basis would set the priority date for the '417 patent at the first time it disclosed "data buffer control signals"—the November 25, 2019 filing date of its application.

Accordingly, Micron respectfully requests that the Court grant summary judgment of lack of written description for the '417 patent.

II. STATEMENT OF ISSUE TO BE DECIDED

A. Whether claim 1 of the '417 patent is invalid for failing to satisfy the written description requirement of 35 U.S.C. § 112, ¶ 1 for the limitation "wherein data transfers through

the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

B. Whether claim 1 of the '417 patent is entitled to a priority date earlier than its filing date for failing to satisfy the written description requirement of 35 U.S.C. § 112, ¶ 1 for the "data buffer control signals" related limitations.

III. STATEMENT OF UNDISPUTED MATERIAL FACTS

A. Asserted Claims of the '417 Patent

1. On November 20, 2023, Netlist served its opening expert report of Dr. William Henry Mangione-Smith regarding, *inter alia*, infringement of the '417 patent, where Dr. Mangione-Smith contended that Micron's DDR4 LRDIMM products practice claims 1-6 and 8-15 of the '417 patent. Ex. A (Mangione-Smith Op. Rpt., Ex. C) at ¶ 1.

2. Claim 1 of the '417 patent requires, *inter alia*, a memory module comprising "circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks" and "wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" (hereinafter the "CAS latency limitation") ECF No. 101-2 ('417 patent), Claim 1.

3. During the *Markman* Hearing, Netlist argued the claims recite a CAS latency requirement for all data transfers, i.e., transfers resulting from both read and write memory commands. Ex. B (*Netlist Inc.*, v. *Samsung Electronics Co., Ltd., et al., Markman* Hearing on September 26, 2023), 111:23-112:2 (Netlist's counsel stating [redacted]

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[redacted]) (emphases added); *see id.*, 111:19-112:22.

4. The Court similarly held in its Claim Construction Order that "[b]ased on the totality of the evidence, a skilled artisan would understand 'CAS latency' ***includes both*** 'read latency' and 'write latency,' depending on the context." ECF No. 228 at 34 (emphases added). The Court explained that the disclosure of the '417 patent:

> explains the one-cycle time delay 'provides sufficient time for *read and write data transfers* to provide the functions of the data path multiplexer/demultiplexer.' . . . Moreover, the disclosure refers to data transfers *between* the memory controller and the memory module rather than in only one direction or the other. . . . Similarly, the claim limitations in which these terms appear refer to . . . 'data transfers *through* the circuitry,' . . .

ECF No. 228 at 33 (emphasis in original).

5. The Court construed the term "overall CAS latency" of a memory module as "the delay between (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module." ECF No. 228 at 36.

6. The Court construed the term "actual operational CAS latency" of a memory device as "the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device." ECF No. 228 at 36.

7. The following is the only discussion of "overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" in the '417 patent:

> In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to

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> the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device 240 does not utilize this extra cycle of time.

ECF No. 101-2 ('417 patent), 22:36-61.

8. The term "data buffer control signals" is found only in the Abstract, Summary of the Invention, and claims of the '417 patent. This term was not provided in prior applications in this patent family. *See* Exhibit C (redline comparison of the '417 patent and its parent U.S. Patent No. 10,89,314) at 1, 3-5.

IV. LEGAL STANDARD

Summary judgment is appropriate when "there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a).

To satisfy the written description requirement of 35 U.S.C. § 112, ¶ 1, the written description "must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (internal quotation marks omitted). The written description requirement "is to ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification." *Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000). This means that all claim limitations, properly construed, must appear in the specification. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d

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1565, 1572 (Fed. Cir. 1997); *see also Hyatt v. Boone*, 146 F. 3d 1348, 1353 (Fed. Cir. 1998). "[A] description which renders obvious a claimed invention is not sufficient to satisfy the written description requirement of that invention." *Regents of the Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1567 (Fed. Cir. 1997). "[T]he hallmark of written description is disclosure. . . . [T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art." *Ariad Pharms.*, 598 F.3d at 1351. The written description requirement is amenable to summary judgment where no reasonable fact finder could return a verdict for the non-moving party. *PowerOasis, Inc. v. T–Mobile USA, Inc.*, 522 F.3d 1299, 1307 (Fed. Cir. 2008) (citing *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1072–73 (Fed. Cir. 2005)); *LizardTech, Inc., v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1346–47 (Fed. Cir. 2005) (affirming summary judgment on invalidity for failure of written description requirement).

V. ARGUMENT

A. Summary Judgment is Warranted on the CAS Latency Limitation

Summary judgment is appropriate because the '417 patent's single-paragraph disclosure for "CAS latency" only discusses adding delay in terms of a register disposed within a memory module adding "one additional clock cycle." Undisputed Material Facts ("UMF") No. 7. This disclosure, however, cannot provide support for the claimed "wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices." This is because "overall CAS latency" (for write command data transfers), under the Court's construction, is determined ***before*** the write command and write data enter a memory module. Thus, the value of the "overall CAS latency" is not affected by registers disposed within a memory module. Similarly, including registers within a memory module could never result in "an overall

CAS latency of the memory module" that is "greater than" an "actual operational CAS latency of each of the memory devices."

More specifically, the '417 patent only includes a single paragraph description with respect to CAS latency delays. UMF No. 7. The paragraph describes including a buffer/register on a memory module to add an "additional clock cycle" that results in an "overall CAS latency of four, and uses memory devices with a CAS latency of three." *Id.*

The '417 patent claims, however, go much further than the description in reciting "wherein data transfers through the circuitry are registered for an amount of time delay ***such that the overall CAS latency*** of the memory module ***is greater than an actual operational CAS latency*** of each of the memory devices." ECF No. 101-2, Claim 1 (emphases added). Netlist argued that the recited instances of CAS latency must be for all data transfers (i.e., resulting from both read and write operations), and the Court, at least in part, agreed. UMF Nos. 3-6. The Court explained that "a skilled artisan would understand 'CAS latency' includes both 'read latency' and 'write latency,' depending on the context" and "the disclosure refers to ***data transfers between*** the memory controller and the memory module ***rather than in only one direction or the other***." UMF No. 4 (emphases added).

The Court then construed the claim term "overall CAS latency" such that the delay for a write data transfer is not affected by registers disposed on a memory module. Specifically, the Court's construction of "overall CAS latency," with respect to write commands, examines the delay between when a write command is made available to a memory module for "execut[ion]" and when the data to be written is made available ***to*** the memory module. That delay necessarily cannot be affected by a register disposed within a memory module—it only involves the delay

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between execution of a write command by a memory module and when the same memory module later receives the data to be written.

The '417 patent's sole disclosure of CAS latency ***at most***, in contrast, relates to read commands and does not provide an adequate written description with respect to transfers going the other way (in response to write commands). For example, the '417 patent describes that "data transfers between the memory controller and the memory module are registered for one additional clock cycle." UMF No. 7. With respect to data read from a memory device, and using the Court's "overall CAS latency" construction discussed above, Netlist may argue that this disclosure supports the claims because a register affects the delay between "the time when a [read] command is executed by a memory module" and when the read data is made available to the memory module. This is because read data from the memory devices has to pass through the register (and thus be delayed by a clock cycle) when being delivered from memory devices to the memory module. Netlist has no argument that this disclosure supports the claims for write data transfers—that support is lacking.

Netlist's expert report provides no valid reason for denying summary judgment. Netlist's expert argues the following:

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Ex. D (Mangione-Smith Reb. Rpt., Exhibit B) at ¶ 87. As shown, Netlist's expert attempts to

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[redacted] *Id.* This is an improper and untimely claim construction position that should be rejected. The '417 patent claim 1 (and the entirety of the intrinsic record) uses the terms "memory module" and "buffer" separately, and there is no basis for equating the two terms as a single thing.

As the Court recognized during claim construction, where Micron argued that CAS latency only applies to a read command, "[w]hile it may be true that, under Netlist's interpretation of 'CAS latency,' the recited limitation can never be met by an accused device, that does not mean the term is indefinite—only that infringement is impossible." ECF No. 228 (Claim Construction Memorandum and Order) at 35. Not only is infringement impossible, the '417 patent fails to disclose any support for the CAS latency limitation with respect to data transfers going to the memory module (write operations) and thus summary judgment is appropriate.

B. The Court Should Grant Summary Judgment That Claim 1 of the '417 Patent is Entitled to a Priority Date No Earlier Than Its Filing Date of November 25, 2019

The '417 patent introduces the concept of "data buffer control signals" for the first time in the application for the '417 patent filed on November 25, 2019. *See* UMF No. 8 and Exhibit C (redline comparison of the '417 patent and its parent U.S. Patent No. 10,89,314) at 1, 3-5. The '417 patent's Abstract recites "[t]he memory module further comprises ***logic configurable to*** receive a set of input address and control signals associated with a read or write memory command and ***output*** registered address and control signals and ***data buffer control signals***," and "[t]he ***circuitry is configurable to enable registered transfers of N-bit wide data signals*** associated with the memory read or write command between the N-bit wide memory bus and the memory devices ***in response to the data buffer control signals*** and in accordance with an overall CAS latency of the memory module. ECF No. 101-2, Abstract. "Data buffer control signals" is only recited three more times in the specification under "Summary of the Invention," merely restating what is recited

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in the Abstract. Specifically, the "Summary of the Invention" states that the logic is further configurable to output data buffer control signals (*id*., 3:50-52), the circuitry is configurable to transfer the burst of data signals in response to the data buffer control signals (*id*., 4:1-4), and "the circuitry is configured to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths" (*id*., 4:24-26). The only time "data buffer control signals" are mentioned again are in the claims.

The '417 patent claims priority to a long series of applications that date all the way back to March 5, 2004. However, these familial patents fail to disclose any "data buffer control signals." *See* Ex. C. While the specification of the '417 patent, and the earlier applications, disclose address signals and control signals, they are separately discussed and claimed from the newly claimed "data buffer control signals." *See, e.g.*, ECF No. 101-2, 16:58-63 (discussing address signals), 9:46-50 (discussing control signals), 42:17-34 (claim 1 reciting "address and control signals"), 42:38-40 (claim 1 reciting "data buffer control signals"). Because the first time "data buffer control signals" are introduced in the written description for the '417 patent is in the November 25, 2019 patent application, the claims of the '417 patent lack written description in its earlier familial patents and is not entitled to claim priority to any earlier date than the filing date of the '417 patent.

VI. CONCLUSION

Thus, for the reasons stated above, Micron respectfully requests that the Court grant its motion for summary judgment that the claims of the '417 patent lack written description.

Dated: January 16, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that, on January 16, 2024, a copy of the foregoing was served on all counsel of record via the Court's ECF system and email.

/s/ Michael R. Rueckheim
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CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this Case.

/s/ Michael R. Rueckheim
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